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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CRAIG, DWIN M	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/469,754	TSUKAMOTO ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☒ Claim(s) *4,12 & 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-39 have been presented for reconsideration in view of Applicant's Request for Reconsideration under 37 C.F.R. 1.114 and Applicant's amended claim language. Claim 40 has been presented for Examination.

Response to Arguments

2. Applicant's arguments filed on 8-25-2004 have been fully considered. Examiners response is as follow:

2.1 Regarding the Applicant's response to the 35 U.S.C. 103 rejections of Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39 over *Bransen et al.* in view of *McNelly et al.*

Applicant argued,

> Since the mega-cell of Brasen has fixed power requirements, no logic simulation is needed for estimation of power consumption by the mega-cell. Brasen simply does not disclose or suggest simulating logic of the mega-cell and estimating power consumed by the mega-cell based on logic simulation. For example, Applicants find no teaching or suggestion in Brasen of determining an alternating current component of power consumed by the mega-cell.

(Page 16 of the 8-25-2004 responses).

The Examiner respectfully points out that the *McNelly et al.* reference was relied upon to disclose the alternating current component limitation. The Applicant is performing *piece meal analysis* of the Examiner's rejections this is a *spurious argument.*

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argued,

> However, Applicants do not find teaching or suggestion in McNelly of simulating logic of a mega-cell and estimating power consumed by the mega-cell based on logic simulation, as described by the claims of this application. For example, Applicants find no teaching or suggestion in McNelly of determining an alternating current component of power consumed by the mega-cell.

(Page 17 of the 8-25-2004 responses)

The Examiner respectfully points out that the *Bransen et al.* reference was relied upon to teach the limitation of simulating a mega-cell. The Applicant is performing *piece meal analysis* of the Examiner's rejections this is a *spurious argument.*

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Further, the Examiner now quotes from the *McNeally et al.* reference **(Col. 1 Lines 39-49):**

> *"Power consumption occurs dynamically (AC)--resulting from the switching of a signal from one voltage level to another, and statically (DC)--when the circuit is "quiet" due to pullups and pulldowns, level shifters, and leakage currents. Most dynamic power consumption is the result of charging and discharging of capacitances in the circuit. Capacitances include pin capacitances, transistor capacitances, and interconnect capacitances. The amount of power consumed by capacitance charging and discharging is represented by the following equation:"*

The Examiner respectfully points out that calculation of an *alternating current (AC) component* of a logic cell is *well* known in the electronic circuit simulation art. The Examiner respectfully points out that the *Bransen et al.* reference discloses the simulation of Mega-cells.

Bransen et al. **(Figures 7 & 8 and Col. 9 Lines 38-48):**

"Referring to FIG. 7, Block 1, Block 2 and Block 3 are physical blocks corresponding to groups of logical elements in an integrated circuit. Each instance 21 corresponds to a logical element. As shown in greater detail in FIG. 8, Block 1 and Block 3 in the present example are composed of combinatorial logic gates. Block 2 is a mega-cell (for example RAM or ROM) having fixed power requirements. The simulation of the power vectors determines the worst-case number of logical elements to be turned on at the same time in each group, allowing accurate power bus widths to be generated."

Applicant has argued that,

Since the mega-cell of Bransen has fixed power requirements, no logic simulation is needed for estimation of power consumption by the mega-cell. Bransen simply does not disclose or suggest simulating logic of the mega-cell and estimating power consumed by the mega-cell based on logic simulation. For example, Applicants find no teaching or suggestion in Bransen of determining an alternating current component of power consumed by the mega-cell.

The Examiner respectfully asserts that, as specifically pointed out in the cited reference above, the *Bransen et al.* reference does teach the simulation of mega-cells and that using fixed power requirements of the mega-cells, *as argued by the Applicant,* is functionally equivalent to the claimed limitations, "*estimating a first value of electric power consumed by said mega cells based on said logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell.*"

The Examiner respectfully asserts that the *fixed power requirements*, as argued, are functionally equivalent to *pre-established power consumption data* as claimed. Further the Examiner respectfully points out that Applicant is claiming, *simulating logic of basic and mega-cells of the integrated circuit,* which is the clearly disclosed in the *Bransen et al.* reference as referred to a *"logic elements"* and *"mega-cells"*, *see* ***Figures 7 & 8 and Col. 9 Lines 38-48*** of *Bransen et al. U.S. Patent 5,481,469.*

The Examiner respectfully refers to *In re Graves (CAFC) 36 USPQ2d 1697 November 9, 1995, No. 95-1199, A reference anticipates a claim if it discloses the claimed invention "such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention."* The Examiner acknowledges that the rejections in this action are directed towards obviousness and not anticipation, however, the *In re Graves,* decision, it is respectfully put forward, illustrates the Examiner's assertions that the claimed subject matter that the Applicant has put forth would be *"obvious"* to a skilled artisan.

The Examiner respectfully asserts that Applicant's arguments, in regards to the 35 U.S.C. 103(a) obviousness rejections of Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39 as being unpatentable over *Bransen et al.* in view of *McNelly et al.* have not been persuasive and the Exmainer upholds these rejections.

2.2 As regards the Applicant's arguments concerning the 35 U.S.C. 103(a) rejections of Claims 1-39 over Raman et al. U.S. Patent 5,535,370 in view of Crafts et al. U.S. Patent 5,521,834 and in further view of Dangelo et al. U.S. Patent 5,493,508.

Applicant argued,

> As acknowledged in the Office Action, Raman does not mention mega-cells and does not disclose or suggest any techniques of calculating the alternating current component of power consumed by mega-cells. Crafts and Dangelo do not cure the deficiencies of Raman.

The Examiner respectfully asserts that applicant's argument is persuasive in that the *Ramen* reference does not expressly disclose *"mega-cells"* where a power analysis of those mega-cells is performed. After a review of the cited art, the Examiner notes that none of the cited references disclose *"mega-cells"* and power analysis and the Examiner withdraws the rejections

based on *Ramen et al., Crafts et al.* and *Dangelo et al.* The Examiner does note however, that the *Dangelo et al.* reference does disclose simulation of *"mega-cells"*.

Claim Objections

3. **Claims 4, 12 and 20** are objected to because of the following informalities: There is no period at the end of the claim. Appropriate correction is required.

Claim Interpretation

4. The Applicant's claim language has been given the broadest reasonable interpretation. For the purposes of examination the examiner has determined that the using of fixed power requirements of the mega-cells, is functionally equivalent to the claimed limitations, "*estimating a first value of electric power consumed by said mega cells based on said logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell.*"

The *fixed power requirements* are functionally equivalent to *pre-established power consumption data*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Independent **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** and dependent **Claim 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Brasen et al. U.S. Patent 5,481,469** in view of **McNelly et al. U.S. Patent 5,625,803.**

5.1 As regards independent **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** the *Brasen et al.* reference discloses, a method of estimating power consumption of an IC **(Col. 1 Lines 28-38),** simulating logic of basic and mega-cells **(Figures 7&8),** estimating a first value of electric power consumed by the mega-cell, with pre-established data **(Block 2 Figure 8 and Figure 6, Col. 3 Lines 14-23).**

The *Bransen et al.* reference discloses the simulation of Mega-cells.

Bransen et al. **(Figures 7 & 8 and Col. 9 Lines 38-48):**

"Referring to FIG. 7, Block 1, Block 2 and Block 3 are physical blocks corresponding to groups of logical elements in an integrated circuit. Each instance 21 corresponds to a logical element. As shown in greater detail in FIG. 8, Block 1 and Block 3 in the present example are composed of combinatorial logic gates. Block 2 is a mega-cell (for example RAM or ROM) having fixed power requirements. The simulation of the power vectors determines the worst-case number of logical elements to be turned on at the same time in each group, allowing accurate power bus widths to be generated."

The Examiner notes that the simulation of power vectors, as disclosed in the cited section of the *Bransen et al.* reference, requires that the, *fixed power requirements,* of the *Block 2 mega-cell* are being used in the simulation that is referred to in the next line, therefore the *Bransen et al.* reference is disclosing that he *fixed power requirements* of the *mega-cells* are being used in the simulation and therefore the *mega-cells* are part of the simulation and therefore the limitation of the *mega-cells* being simulated is being disclosed.

As regards the claimed limitation, simulating logic of basic and mega-cells of the integrated circuit, these limitations are clearly disclosed in the Bransen et al. reference and are referred to as "logic elements" and "mega-cells", see **Figures 7 & 8 and Col. 9 Lines 38-48** of the Bransen et al. reference.

However, the *Brasen et al.* reference does not expressly disclose calculation of alternating current component.

The *Brasen et al.* reference discloses that there is a need in the art for accurate calculation of the power dissipation of logic elements **(Col. 2 Lines 1-4).** An artisan of ordinary skill, would have been motivated, to search the electronic design arts to find a method of accurate calculation of the power dissipation of logic elements as suggested by the *Brasen et al.* reference. In the integrated circuit design art, the *McNelly et al.* reference discloses a method of accurate calculation of the power dissipation of logic elements, specifically the alternating current component **(Figure 7, Col. 2 Lines 32-38).**

Further, the Examiner now quotes from the *McNeally et al.* reference **(Col. 1 Lines 39-49):**

"Power consumption occurs dynamically (AC)--resulting from the switching of a signal from one voltage level to another, and statically (DC)--when the circuit is "quiet" due to pullups

and pulldowns, level shifters, and leakage currents. Most dynamic power consumption is the result of charging and discharging of capacitances in the circuit. Capacitances include pin capacitances, transistor capacitances, and interconnect capacitances. The amount of power consumed by capacitance charging and discharging is represented by the following equation:"

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the integrated circuit power estimation methods of the *Brasen et al.* reference with the integrated circuit power estimation methods of the *McNelly et al.* reference because, the use of the methods disclosed in the *McNelly et al.* reference will provide for more accurate power consumption data for IC design and thus provide the designer with a model of how the finished IC will perform **(McNelly et al. Col. 2 Lines 33-46).**

5.2 As regards dependent **Claim 40** the *Brasen et al.* reference discloses a predetermined constant value; *Block 2 is a mega-cell (for example RAM or ROM) having fixed power requirements* ***Col. 9 Lines 38-48.*** The Examiner asserts that a *fixed power requirement* is functionally equivalent to a predetermined constant value.

However the *Brasen et al.* reference does not expressly disclose an alternating current component consumed by *a logic element,* for each logic state is determined by utilizing a predetermined constant value and the average operation frequency for the logic state.

The *McNelly et al.* reference discloses a *predetermined constant value* **(Col. 9 Lines 63-67 & Col. 10 Lines 1-10),** where the current consumed by the mega cells for each logic state is determined **(Figure 8** displays a *histogram* where there are different logic states disclosed, further, it is noted by the Examiner that the CIR calculation, as disclosed in the *McNelly et al.* reference discloses calculations of AC power consumption of a *cell* or *unit* in a

logic simulation during the transition from logic low to logic high **(Col. 6 Lines 60-67, Col. 7 Lines 1-67 and Col. 8 Lines 1-11))**, and determining the power consumed by the logic gate based on the frequency for the logic state **(Col. 1 Lines 40-55, *note in the formula the term labeled "FREQUENCY"*).**

It would have been obvious, to one of ordinary skill in the art, to have used the methods of AC power consumption modeling of a logic gate as disclosed in the *McNelly et al.* reference because the improved methods disclosed in the *McNelly et al.* reference provide for more accurate power consumption data for IC design and thus provide the designer with a model of how the finished IC will perform **(McNelly et al. Col. 2 Lines 33-46).**

6. Dependent **Claims 2-8, 10-16, 18-23, 26-28, 30-32 and 34-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Brasen et al. U.S. Patent 5,481,469** in view of **McNelly et al. U.S. Patent 5,625,803** and in further view of *"OFFICIAL NOTICE"*.

6.1 As regards independent **Claims 1, 9, 17, 25, 29 and 33** please see section **5.1** above.

6.2 As regards dependent **Claims 2-8, 10-16, 18-23, 26-28, 30-32 and 34-36** all of the limitations of these claims are directed to different computer readable media comprising, floppy disks, CDROM, DVD and other known in the art methods of recording computer data.

From **MPEP section 2144.03** is stated,

Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known.

The Examiner notes the following: this office action is NOT a final office action and the use of floppy disks, CDROM's, DVD's and compression technology used on storage media are all common knowledge in the computer data storage art in which the Examiner could provide instant and unquestionable demonstration of being well-known.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have used floppy disks, CDROM recorded media, DVD recorded media, as well as compression technology because, these are methods, known in the art, of storing and transferring data on computer systems that have established standards.

Conclusion

7. **Claims 1-40** are rejected.

7.1 This action is **NON-FINAL.**

7.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (571)272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-305-7150.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC